Remarks/Arguments

Claim 7 is amended to clarify that conductive vias are formed in the blind vias (as shown in FIG. 3C), and the first and second resist layers and parts of the conductive film covered by the first resist layer are removed after forming the metal barrier layer (as supported by FIGs. 3E to 3H and page 12 of the specification). Amended claim 14 recites the use of the same resist layer for the first and second electroplating processes and formation of a metal barrier layer on the contact pads in the openings of the resist layer, as shown in FIG. 4.

The rejection of independent claims 7 and 14, and dependent claims 8, 10, 11, 12, 15, 16, 18, 19, and 20 under 35 U.S.C. § 102(a) as being anticipated by Makino et al. (US 6,566,239) (hereinafter Makino) is respectfully traversed. As an initial matter, a comparison of claim 7 to the method disclosed in Figures 1 – 10 of Makino demonstrates that the Makino invention and the instant invention belong to different technical fields and have different technical contents, to wit:

Claim 7 of the present invention is directed to a fabrication method for a semiconductor package substrate having a contact pad protective layer formed thereon. The method comprises the steps of:

S1: providing an insulating layer having a plurality of blind vias formed therein for exposing inner traces disposed underneath the insulating layer;

S2: forming a conductive film on the insulating layer and over the blind vias;

S3: forming a first resist layer on the conductive film, wherein the first resist layer has a plurality of openings to expose predetermined parts of the conductive film;

S4: performing a first electroplating process to form a patterned trace layer in the openings and form conductive vias in the blind vias, wherein the patterned trace layer comprises a plurality of contact pads, and at least one

of the contact pads is electrically connected to at least one of the conductive vias;

S5: forming a second resist layer over the patterned trace layer exclusive of the contact pads, making the contact pads exposed from the second resist layer;

S6: performing a second electroplating process to form a metal barrier layer on the contact pads; and

S7: after forming the metal barrier layer, removing the second resist layer, the first resist layer, and parts of the conductive film covered by the first resist layer.

On the other hand, the method disclosed in FIGS. 1-10 of Makino comprises the steps of:

FIG. 1: forming an insulating film 13 on a wafer 11 having an electrode pad 12, with the electrode pad 12 being exposed from the insulating film 13, and forming a metal film 14 on the insulating film 13 and the electrode pad 12;

FIG. 2: providing a first resist 15 on the metal film 14, and forming an opening 16 in the first resist 15 to expose a part of the metal film 14;

FIG. 3: performing an electroplating process to form a wiring film 17 in the opening 16 of the first resist 15;

FIG. 4: removing the first resist 15;

FIG. 5: providing a second resist 18, and forming an opening 19 in the second resist 18 to expose a part of the wiring film 17;

FIG. 6: performing the electroplating process to form a post 20 in the opening 19 of the second resist 18;

FIG. 7: performing the electroplating process to form an Ni film 21 on the post 20;

FIG. 8: performing the electroplating process to form an Au film 22 on the Ni film 21;

FIG. 9: removing the second resist 18; and

FIG. 10: removing the metal film 14 underlying the resist 18.

The following comments compare the above two methods:

(1) Comparing S1, S2 of the present application and FIG. 1 of Makino, since the present application is used for fabrication of a package substrate, it is necessary to form blind vias in the insulating layer so as to expose inner traces disposed underneath the insulating layer; however, Makino is to perform fabrication processes on a wafer without having to form blind vias, and only the wafer surface is subjected to the fabrication processes.

(2) Comparing S2-S4 of the present application and FIGs. 2-3 of Makino, since the present application is used for fabrication of a package substrate, it is necessary to simultaneously form a patterned trace layer on the insulating layer and form conductive vias in the blind vias during the electroplating process; however, Makino is to perform fabrication processes on a wafer without having to form blind vias, and the wiring structure formed in the electroplating process thereof is only formed on a surface of the insulating film of the wafer.

(3) Comparing S5 of the present application and FIGS. 4-5 of Makino, the present application directly forms a second resist layer on the first resist layer, the second resist layer covering the patterned trace layer exclusive of the contact pads, making the contact pads exposed from the second resist layer; however in Makino, the first resist is removed firstly, and then the second resist is provided and is formed with an opening for exposing a part of the wiring film.

(4) Comparing S6 of the present application and FIGS. 6-8 of Makino, the present application directly electroplates a metal barrier layer such as nickel, gold on the contact pads; however, Makino electroplates firstly the post and then the Ni film and Au film.

(5) Comparing S7 of the present application and FIGS. 9-10 of Makino, the present application removes the first and second resist layers in the same process; however, Makino removes the first resist before forming the second resist, such that the first resist and the second resist are removed by different multiple processes.

Therefore, by the above detailed comparison between the steps for fabricating a package substrate in claim 7 of the present application and the fabrication processes of Makino (FIGs. 1-10), the invention of the present application and that of Makino are seen to belong to different technical fields and have different technical contents.

Turning now more directly to the rejection, the invention cannot be viewed as anticipated, or obvious over, Makino. Makino discloses a wafer-level technique, which is different from the technical field of the present application for fabricating a semiconductor package substrate. Makino does not teach or suggest forming blind vias in the insulating layer of the substrate, and performing a first electroplating process to form a patterned trace layer on the insulating layer and form conductive vias in the blind vices of the insulating layer, as defined in independent claims 7 and 14 of the present application.

The method recited in claim 7 of the present application is not disclosed or taught by Figs. 1-12 of Makino. By the above amendment, the first and second resist layers in the present application are both removed in the same step after forming the metal barrier layer, as shown in FIG. 3G (page 12, lines 19-12). However, in Makino, the first resist 15 is removed after forming the wiring film 17 as shown in Figs. 3-4 and before forming the second resist 18 in Fig. 5; subsequently, the second resist layer 18 is removed as shown in Figs. 8-9. Makino does not teach or suggest removing both the first and second resist layers after forming the metal barrier layer. The present application uses the same removing process to remove both the first and second resist layers, which cannot be anticipated by the different processes for separately removing the first resist 15 and the second resist 18 in Makino. As a result, the present application is able to reduce the processing time and processing costs as compared to Makino.

The method-recited in claim 14 of the present application is not disclosed or taught by Figs. 1-12 of Makino. As discussed above, Makino uses two resists 15 and 18, which are separately formed and separately removed. However, the method in claim 14 of the present application, as shown in FIG. 4, uses the same resist layer 32 for the first and second electroplating processes and forms the metal barrier layer on the contact pads 330 in the openings of the resist layer 32. Such method is not disclosed or taught by Makino.

In conclusion, Makino cannot anticipate the methods recited in claims 7 and 14 of the present application, such that claims 7 and 14 are novel over Makino. Thus, the dependent

claims of claims 7 and 14 are also patentable over Makino or further in view of the other cited prior arts.

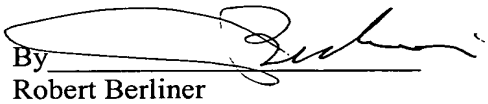
The rejections of claims 9 and 17 under 35 U.S.C. § 103(a) as unpatentable over Makino in view of Shinomiya (5,907,786), and of claim 13 under 35 U.S.C. § 103(a) as unpatentable over Makino in view of Wang et al. (2004/0000427) are both respectfully traversed. In light of the differences between Makino and the present invention, as described above, combination with either Shinomiya or Wang et al. still fails to teach or suggest a inventive and useful fabrication method of a semiconductor package substrate having contact pad protective layer formed thereon. Furthermore, one skilled in the art might lack motivation or disable to deduct those characteristic inventive steps of the present invention from these reference documents.

Applicants believe the application is in condition for allowance and respectfully solicit a Notice of Allowance.

The Commissioner is hereby authorized to charge any fee which should have been filed herewith to our Deposit Account No. 50-0337, under Order No. 7452-105/10313554. A duplicate copy of this paper is enclosed.

Dated: August 23, 2005

Respectfully submitted,



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